

United States Patent and Trademark Office

UNITED STATES DEPARTMENT OF COMMERCE United States Patent and Trademark Office Address: COMMISSIONER FOR PATENTS P.O. Box 1450 Alexandria, Virginia 22313-1450 www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.		
09/362,041	07/28/1999	SEIICHI SAITOH	500.37414X00	6332		
20457	7590 12/18/2003	EXAMINER				
ANTONELLI, TERRY, STOUT & KRAUS, LLP 1300 NORTH SEVENTEENTH STREET			HUA, LY			
SUITE 1800		ART UNIT	PAPER NUMBER			
ARLINGTON, VA 22209-9889			2135	6		
			DATE MAILED: 12/18/2003	, p		

Please find below and/or attached an Office communication concerning this application or proceeding.

	Application N .	Applicant(s)							
	09/362,041	SAITOH ET AL.							
Offic Action Summary	Examin r	Art Unit							
	Ly V. Hua	2131							
The MAILING DATE of this communication app Period for Reply	pears n the cover sheet with the	correspondence address							
A SHORTENED STATUTORY PERIOD FOR REPL' THE MAILING DATE OF THIS COMMUNICATION. - Extensions of time may be available under the provisions of 37 CFR 1.1 after SIX (6) MONTHS from the mailing date of this communication. - If the period for reply specified above is less than thirty (30) days, a reply - If NO period for reply is specified above, the maximum statutory period of the period of the period for reply within the set or extended period for reply will, by statute - Any reply received by the Office later than three months after the mailing earned patent term adjustment. See 37 CFR 1.704(b). Status	36(a). In no event, however, may a reply be to y within the statutory minimum of thirty (30) dawill apply and will expire SIX (6) MONTHS from the application to become ABANDON	imely filed ays will be considered timely. In the mailing date of this communication. ED (35 U.S.C. § 133).							
1) Responsive to communication(s) filed on									
2a) This action is FINAL . 2b) This	☐ This action is FINAL . 2b)☐ This action is non-final.								
3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under <i>Ex parte Quayle</i> , 1935 C.D. 11, 453 O.G. 213.									
Disposition of Claims									
 4) Claim(s) 1-8 is/are pending in the application. 4a) Of the above claim(s) is/are withdraw 5) Claim(s) is/are allowed. 6) Claim(s) is/are rejected. 7) Claim(s) is/are objected to. 8) Claim(s) 1-8 are subject to restriction and/or el 									
Application Papers									
9) The specification is objected to by the Examine 10) The drawing(s) filed on is/are: a) acc Applicant may not request that any objection to the Replacement drawing sheet(s) including the correct	epted or b) objected to by the drawing(s) be held in abeyance. So tion is required if the drawing(s) is o	ee 37 CFR 1.85(a). bjected to. See 37 CFR 1.121(d).							
11) ☐ The oath or declaration is objected to by the Ex Priority under 35 U.S.C. §§ 119 and 120	kammer. Note the attached Offic	e Action of form PTO-152.							
12) Acknowledgment is made of a claim for foreign a) All b) Some * c) None of: 1. Certified copies of the priority document 2. Certified copies of the priority document 3. Copies of the certified copies of the priority document application from the International Bureau * See the attached detailed Office action for a list 13) Acknowledgment is made of a claim for domesti since a specific reference was included in the first 37 CFR 1.78. a) The translation of the foreign language pro 14) Acknowledgment is made of a claim for domesti reference was included in the first sentence of the	is have been received. Is have been received in Applica rity documents have been received (PCT Rule 17.2(a)). In of the certified copies not received priority under 35 U.S.C. § 119 st sentence of the specification of the certified copies ic priority under 35 U.S.C. § 12 points application has been residually under 35 U.S.C. §§ 12	tion No yed in this National Stage red. (e) (to a provisional application) or in an Application Data Sheet. sceived. 0 and/or 121 since a specific							
Attachment(s)	_								
1) Notice of References Cited (PTO-892) 2) Notice of Draftsperson's Patent Drawing Review (PTO-948) 3) Information Disclosure Statement(s) (PTO-1449) Paper No(s)	5) Notice of Informal	y (PTO-413) Paper No(s) Patent Application (PTO-152)							

Election/Restriction

1. Restriction to one of the following inventions is required under 35 U.S.C. 121: Group I a. Claims 1 ans 2, ii. drawn to: (1)1a digital signal processing apparatus connected to other digital signal processing apparatuses (i) (ii) by means of a digital signal bus to transmit/receive a digital signal, (b) wherein said digital signal processing apparatus comprises (i) an interface circuit so that when said digital signal processing apparatus is powered on, said interface circuit performs authentication between [1]said digital signal processing apparatus and [2] any of said other digital signal processing apparatuses [a] powered on simultaneously with or [I] before power-on of said digital signal processing apparatus; and (2)2a digital signal processing apparatus (a) connected to other digital signal processing apparatuses (i) (ii) by means of a digital signal bus to transmit/receive a digital signal, (b) wherein said digital signal processing apparatus comprises an interface circuit (i) so that when powering-on of said other digital signal processing apparatuses is detected, said interface circuit performs authentication between [1] said digital signal processing apparatus [2] any of said other digital signal processing apparatuses; iii. classified in class 713, subclass 200. b. Group II Claims 3 and 5, ii. drawn to: (1)3a digital signal processing apparatus connected (a) to other digital signal processing apparatuses (ii) by means of a digital signal bus to transmit/receive a digital signal, (b) wherein said digital signal processing apparatus comprises an interface circuit (i) which performs authentication between said digital signal processing apparatus and said other digital signal processing apparatuses II when said interface circuit is connected to said digital signal bus; and (2)5a digital signal processing apparatus provided with (a) a plurality of input terminals including an input terminal 1)

(b)

connected

from a digital signal bus and

(i)

```
by means of said digital signal bus
                                         (ii)
                                                   1)
                                                              to transmit/receive a digital signal,
                               (c)
                                         wherein said digital signal processing apparatus comprises:
                                                   a switching circuit
                                         (i)
                                                              for selecting
                                                   1)
                                                                        said plurality of input terminals; and
                                         (ii)
                                                   an interface circuit
                                                   1)
                                                              which performs authentication between
                                                                        said digital signal processing apparatus and
                                                              II
                                                                        said other digital signal processing apparatuses
                                                             Ш
                                                                        when said input terminal connected to said digital
                                                                        signal bus is selected by said switching circuit; and
                    classified in class 713, subclass 200.
          iii.
c.
          Group III
                    Claim 4,
          ii.
                    drawn to:
                    (1)4
                               a digital signal processing apparatus
                                         connected
                                                   to other digital signal processing apparatuses
                                         (i)
                                                   by means of a digital signal bus
                                         (ii)
                                                             to transmit/receive a digital signal,
                               (b)
                                         wherein said digital signal processing apparatus comprises
                                                   an interface circuit
                                         (i)
                                                              which performs authentication between
                                                                        said digital signal processing apparatus and
                                                                        said other digital signal processing apparatuses
                                                             II
                                                             Ш
                                                                        when connection
                                                                        [1]
                                                                                  of said other digital signal processing
                                                                                  apparatuses
                                                                        [2]
[3]
                                                                                  to said digital signal bus
                                                                                  is detected; and
          iii.
                    classified in class 713, subclass 200.
d.
          Group IV
                    Claim 6,
          ii.
                    drawn to:
                    (1)6
                               a digital signal processing apparatus
                                         connected
                                         (i)
                                                   to other digital signal processing apparatuses
                                         (ii)
                                                   by means of a digital signal bus
                                                   1)
                                                             to
                                                                        encrypt a digital signal and
                                                             Ī
                                                             II
                                                                       transmit/receive said encrypted digital signal,
                                         wherein said digital signal processing apparatus comprises:
                              (b)
                                                   an interface circuit
                                         (i)
                                                             which performs authentication between
                                                   1)
                                                                        said digital signal processing apparatus and
                                                                        said other digital signal processing apparatuses; and
                                         (ii)
                                                   a storage circuit for storing
                                                             a key used to decrypt
                                                   1)
                                                                        said encrypted digital signal
                                                                                  which is subjected to
                                                                                  transmission/reception of between
                                                                                            said digital signal processing
                                                                                  [a]
                                                                                            apparatus and
                                                                                            each of said other digital signal
                                                                                  [b]
                                                                                            processing apparatuses; and
          iii.
                    classified in class 713, subclass 168.
          Group V
e.
                    Claim 7,
          ii.
                    drawn to:
                              a digital signal processing apparatus
                    (1)7
```

to other digital signal processing apparatuses

Art Unit: 2131

		(a)	connected						
			(i)	 (i) to other digital signal processing apparatuses (ii) by means of a digital signal bus 					
			(ii)		s of a digi having	tal signal	bus		
				1)		I a plurality of transmission channels			
					II	to thereby			
						[1]	encrypt [a] [b]	a digital signal in accordance with copyright control information of said digital signal and	
						[2]	perform	signal and	
						. ,	[a]	transmission/ reception of said encrypted digital signal,	
		(b)			al signal processing apparatus comprises				
			(i)	an interf	ace circuit which cl				
				• ,	I		nsmission o	channels of said digital signal bus	
								said copyright control information	
		.1	- 712 - 1	-1 160	Ш	when sa	aid digital s	signal is to be transmitted; and	
	iii.	classified in clas	s /13, sub	ciass 168.					
f.	Group \ i. ii.	VI Claim 8, drawn to:							
	11.		al signal pr	rocessing ap	paratus				
		(a)	connec	ted	•				
	•		(i)				ssing appar		
		(b)	(ii) wherei	oy mean n said digita				hange a digital signal,	
		(0)	(i)	a circuit			ирригити	Comprises	
				1)	for defin				
					1	a name and	of said dig	ital signal processing apparatus	
					II		of said othe	r digital signal processing	
						apparat	uses		
	iii.	classified in clas	s 713, sub	class 200.		[2]	connecte	ed to said digital signal bus; and	

Inventions of Groups I to V and VI are related as subcombinations disclosed as usable together in a single combination. The subcombinations are distinct from each other if they are shown to be separately usable. In the instant case, invention of Groups I to V and VI has separate utility such as presented as follow. See MPEP § 806.05(d).

In the instant case, invention of each of the Groups I to V and VI has separate utility such as presented as follow:

i. The invention of Group I (claims 1 and 2) has a usage of authenticating between one digital signal processing apparatus and other digital signal processing apparatuses when a digital signal processing apparatus is powered on, which utility is not needed for any of the other invention of the other Groups.

ii. The invention of Group II (claims 3 and 5) has a usage of authenticating between one digital signal processing apparatus and other digital signal processing apparatuses when an authenticating entity residing in the one digital signal processing apparatus is connected to a bus, which utility is not needed for any of the other invention of the other Groups.

iii. The invention of Group III (claim 4) has a usage of authenticating between one digital signal processing apparatus and other digital signal processing apparatuses when the other digital signal processing apparatuses are connected to a bus, which utility is not needed for any of the other invention of the other Groups.

The invention of Group IV (claim 6) has a usage of storing a key used to decrypt digital signal, which iv. utility is not needed for any of the other invention of the other Groups.

The invention of Group V (claim 7) has a usage of changing (1) transmission channels of a digital signal bus

- (2) in accordance with copyright control information
- when a digital signal is to be transmitted, (3)

which utility is not needed for any of the other invention of the other Groups.

The invention of Group VI (claim 8) has a usage of defining vi.

a name of said digital signal processing apparatus and (1)

Application/Control Number: 09/362,041

Art Unit: 2131

- (2) names of said other digital signal processing apparatuses, which utility is not needed for any of the other invention of the other Groups.
- 3. Because these inventions are distinct for the reasons given above and the search required for one Group is not required for any of the other Groups, restriction for examination purposes as indicated is proper.
- 4. A telephone call was made to Mr. Carl Brundidge (Reg. No. 29,621) on September 30, 2003, to request an oral election to the above restriction requirement, but did not result in an election being made

Applicant is advised that the reply to this requirement to be complete must include an election of the invention to be examined even though the requirement be traversed (37 CFR 1.143).

- 5. Applicant is reminded that upon the cancellation of claims to a non-elected invention, the inventorship must be amended in compliance with 37 CFR 1.48(b) if one or more of the currently named inventors is no longer an inventor of at least one claim remaining in the application. Any amendment of inventorship must be accompanied by a request under 37 CFR 1.48(b) and by the fee required under 37 CFR 1.17(I).
- 6. Any response to this action should be mailed to:

Commissioner of Patents and Trademarks Washington, D.C. 20231

or faxed to:

(703)872-9306, (for formal communications intended for entry)

or:

(703) 872-9306 (for informal or draft communications, please label "PROPOSED" or "DRAFT")

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington. VA., Sixth Floor (Receptionist).

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Examiner Ly Hua whose telephone number is (703) 305-9684. The examiner can normally be reached on Monday to Friday from 9:30 AM to 6:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sheikh, Ayaz, can be reached on (703) 305-9648. The fax phone number for this Group is (703) 305-3718.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 305-9600.

LY V. HUA PRIMARY PATENT EXAMINER ART UNIT 2131

L. Hua October 22, 2003